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Remarks

Thorough examination by the Examiner is noted and appreciated.

Claim Rejections under 35 USC 103

1. Claims 1, 9, 19, and 21 stand rejected under 35 USC 103(a) as being unpatentable over Guo (US 6,596,599) in view of Hsiao et al (US PUB 2004/0241920) as evidenced by a copy of a" Glossary for Intel's high0-K, Metal gate Transistor announcement" hand dated 4/1/2004.

Statement of Common Ownership Pursuant to 35 USC 103(c)

Applicants' attorney of record states that Guo (US 6,596,599 B1) and Applicants instant application were, at the time the invention was made, owned by Taiwan Semiconductor Manufacturing Company. Therefore, Examiners use of Guo (US 6,596,599 B1), which qualifies as prior art under section 102(e) as a reference in a 103(a) rejection appears to be improper under 35 USC §103(C). See e.g., MPEP 706.02(l).

However, while not agreeing Guo may be properly be used as a

reference in a rejection under 103(a), assuming *arguendo* that it is a properly used reference, Applicants respectfully traverse Examiner's rejection under 35 U.S.C. 103(a).

Guo discloses a method for forming a gate structure that includes a high-K gate dielectric, a pre-doped polysilicon gate electrode and where capacitive coupling between the source/drain regions is minimized by gate spacers that contain an air gap (see Abstract; col 2, lines 25-28). Guo teaches that the threshold Voltage of the device is determined by the source to channel interface (col 4, lines 41-43). Guo teaches forming the high-K gate dielectric (52; Fig 4) over a buffer layer by an LPCVD process (col 5, lines 31-35; lines 64-67). Guo teach forming a bottom gate layer (54) and a top gate layer (56) of doped and undoped polysilicon, respectively. Guo teaches forming an undercut in the bottom gate layer (54; Figure 5) during a gate etching process.

Guo teaches a significantly different structure to overcome a completely different problem than Applicants disclosed and claimed invention.

It is also noted that Guo nowhere discusses interface states

between a high-K gate dielectric and a gate electrode. Further Intel nowhere discusses interface states between a high-K gate dielectric and a gate electrode, but like Applicants discuss in the background, allows a thicker gate dielectric to be formed compared to SiO2, which reduces current leakage (see Applicant Specification at paragraph 003 and Intel's definition of High-K material and Leakage (2d page).

In further contrast, Hsiao discloses a method of fabricating a thin-film transistor (TFT) (for use in liquid crystal displays), a significantly different structure than Guo (see Abstract; paragraphs 002, and 006). For example, a gate metal (Fig 2, 202) (paragraph 0028) is formed **on a substrate** (201) **(glass or quartz)** or a color filer (see paragraphs 0012, 0029). The metal gate is then subjected to an H2 plasma, followed by forming a gate insulating film (204; Fig 2) the metal gate (paragraphs 0011, 0012, 0036). A semiconductor layer (Fig 2, 205) is then deposited on the insulating film (paragraph 0037) Pretreatment of the gate metal prior to deposition of the gate insulator prevents peeling of the insulator (paragraph 0011).

Thus, the fact that Hsiao discloses a H2 plasma treatment of a gate metal in a completely unrelated structure, and where it is

unclear where the H2 plasma treatment of Hsiao would take place in the unrelated structure of Gao (where a gate dielectric is formed over a semiconductor substrate and a gate electrode (polysilicon) formed on the gate dielectric) does not provide motivation to modify Gao since Gao nowhere teaches a metal gate electrode or an overlying insulating layer on the gate electrode that would have improved adhesion due to any such H2 plasma treatment as taught by Hsiao.

Nevertheless, even assuming arguendo, a proper motivation for combination, such combination does not produce Applicants disclosed and claimed invention.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

"The prior art must provide a motivation or reason for the worker in the art, without the benefit of appellant's specification, to make the necessary changes in the reference device." *Ex parte Chicago Rawhide Mfg. Co., 223 USPQ 351, 353*

(Bd. Pat. App. & Inter. 1984).

2. Claims 2-4, 13-15, and 22 stand rejected under 35 USC 103(a) as being unpatentable over Guo and Hsiao et al., above and further in view of both Teng et al. (US 6,797,576) (US PUB 2004/0241920) and Wolf (Silicon Processing for the VLSI Era Vol 1; Process Technology; pg 58, para 2, 1986, Lattice Press).

Applicants reiterate the comments made above with respect to Guo and Hsiao et al.

Even assuming arguendo a proper motivation for combination, the further fact that Teng discloses a method for forming an IGFET where the source and drain regions are formed with a more lightly doped region underneath a normally doped region and where and an anneal in N2 (non-reactive) or oxygen containing ambient is carried out to repair lattice damage **in the semiconductor substrate** induced by the source/drain ion implantation as well as activate the dopants, and where the gate dielectric is a composite silicon oxynitride/silicon dioxide layer, does not further help Examiner in producing Applicants invention.

The **semiconductor structure is now thermally annealed to repair lattice damage and activate the implanted source/drain and halo dopants.** The anneal, referred to as the source/drain-halo anneal, is of such a nature that, at the end of the anneal, gate electrode 88 (68) extends slightly over source/drain extensions 80E and 82E (160E and 162E), and gate electrode 168 (148) extends slightly over source/drain extensions 160E and 162E (140E and 142E).

The source/drain-halo anneal is typically an RTA at 1000-1100.degree., typically 1075.degree. C., for 5-20 sec., preferably 10-15 sec., typically 12 sec. The RTA typically includes a ramp-up from 525.degree. C. to the anneal temperature at 60-90.degree. C./sec., typically 75.degree. C./sec. The RTA also typically includes a ramp-down from the anneal temperature to 700.degree. C. at -40--60.degree. C./sec., typically -50.degree. C./sec. The RTA is **preferably done in an non-reactive environment, typically nitrogen. Alternatively, the RTA can be done in a reactive oxygen-containing environment. In this case, silicon oxide grows along the upper silicon (both monosilicon and polysilicon) surfaces.** The so-grown oxide can replace the capping dielectric layer.

Further, even assuming arguendo, a proper motivation for combination, the additional fact that Wolf discloses that RTP systems are conventionally used in semiconductor processing and that heating is typically done in inert atmospheres including Ar or N2 or vacuum may be used or oxygen or ammonia for growth of SiO2 and Si3N4 (page 58, first paragraph) as well as generally disclosing that temperatures may range from 420 to 1150 °C, depending of the process, and further note that RTP is used to activate dopants after ion implantation and that new

applications for the technique are constantly being discovered (3d paragraph). does not further help Examiner in producing Applicants invention..

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

3. Claims 5, 7, 16, and 18 stand rejected under 35 USC 103(a) as being unpatentable over Guo and Hsiao et al., above and further in view of Shinriki et al. (2005/0074983).

Applicants reiterate the comments made above with respect to Guo and Hsiao et al.

Applicants note that Shinriki et al. teach an apparatus for atomic layer deposition and further teach:

[0006] In order to form such a high-K dielectric gate insulation film on a Si substrate, there is a need of forming an SiO.sub.2 film having a thickness 1 nm or less, typically 0.8 nm or less, on the Si substrate as a base oxide film so as to suppress

diffusion of metal elements constituting a high-K dielectric gate insulation film into the Si substrate, and then form a high-K dielectric gate insulation film on such extremely thin SiO.sub.2 base oxide film. **Thereby, the high-K dielectric gate insulation film has to be formed such that the film does not contain defects such as interface states. Further, at the time of forming such a high-K dielectric gate insulation film on the base oxide film, it is preferable to change the composition thereof gradually from the composition primarily of SiO.sub.2 to the composition primarily of the high-K dielectric, from the side thereof contacting with the base oxide film toward the principal surface of the high-K dielectric gate insulation film.**

[0007] In order to form the high-K dielectric gate insulation film such that it does not contain defects, it is not possible to use plasma process that involves the process of charged particles. For example, when such a high-K dielectric gate insulation film is formed by a plasma CVD process, there are formed defects that function as the trap of hot carriers within the film as a result of the plasma damages.

Even assuming arguendo a proper motivation for combining the base oxide and high-K dielectric layer formation process of Shinriki et al. to form the base layer and high-K dielectric layer of Guo, such modification does not produce Applicants invention, including "A method for treating a gate structure comprising a high-K gate dielectric stack **to reduce interface states between a high-K gate dielectric and a gate electrode**".

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior

art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

4. Claim 6 stands rejected under 35 USC 103(a) as being unpatentable over Guo and Hsiao et al., above and further in view Haukka et al. (2002/0115252).

Applicants reiterate the comments made above with respect to Guo and Hsiao et al.

Even assuming *arguendo,* a proper motivation for combination, the further fact that Haukka et al. teach a high-K dielectric, including hafnium oxide, sandwiched between two aluminum oxide layers or lanthanide oxide layers (see Abstract), does not further help Examiner in producing Applicants invention.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

5. Claim 8 stands rejected under 35 USC 103(a) as being

unpatentable over Guo and Hsiao et al., above and further in view Sarigiannis et al. (2004/0152304).

Applicants reiterate the comments made above with respect to Guo and Hsiao et al.

Even assuming *arguendo*, a proper motivation for combination, the further fact that Sarigiannis et al. teach a method for reducing the purge time of reactive species in an ALD process by placing a high temperature surface in the reactor to destroy the active species during purging to reduce a purge time, (see Abstract), does not further help Examiner in producing Applicants invention.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

6. Claims 11 and 20 stand rejected under 35 USC 103(a) as being

unpatentable over Guo, Hsiao et al., and Shinriki et al., above and further in view Steger (5,085,727).

Applicants reiterate the comments made above with respect to Guo, Hsiao et al., and Shinriki et al.

Even assuming *arguendo*, a proper motivation for combination, the further fact that Steger generally teach a **plasma etcher** may operated over a broad range of pressures depending on the plasma etcher, and without respect to any particular process, does not further help Examiner in producing Applicants invention.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

"we do not pick and choose among the individual elements of assorted prior art references to recreate the claimed invention,

but rather we look for some teaching or suggestion in the references to support their use in a particular claimed combination". Symbol Technologies, Inc. v. Opticon, Inc., 935 F.2d 1569, 19 USPQ2d 1241 (Fed. Cir. 1991).

Conclusion

The multiplicity of cited references, singly or in combination, do not disclose or suggest Applicants disclosed and claimed invention and therefore fail to make out a *prima facie* case of obviousness.

Based on the foregoing, Applicants respectfully submit that the Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in condition for allowance for any reason, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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